

# **EXHIBIT F**

DOCKET NO.: 1745950-00120US1

Filed on behalf of STMicroelectronics, Inc.

By: Richard Goldenberg, Reg. No. 38,895 (Lead Counsel)  
Gregory Lantier (*pro hac vice* to be filed) (Backup Counsel)  
Scott Bertulli, Reg. No. 75,886 (Backup Counsel)  
Trishan Efram, Reg. No. 74,075 (Backup Counsel)  
Wilmer Cutler Pickering Hale and Dorr LLP  
60 State Street  
Boston, MA 02109  
Email: richard.goldenberg@wilmerhale.com  
gregory.lantier@wilmerhale.com  
scott.bertulli@wilmerhale.com  
trishan.esram@wilmerhale.com

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

STMICROELECTRONICS, INC.  
Petitioner

v.

THE TRUSTEES OF PURDUE UNIVERSITY  
Patent Owner

IPR2022-00252  
U.S. Patent No. 7,498,633

**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. 7,498,633  
CHALLENGING CLAIMS 9–11  
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

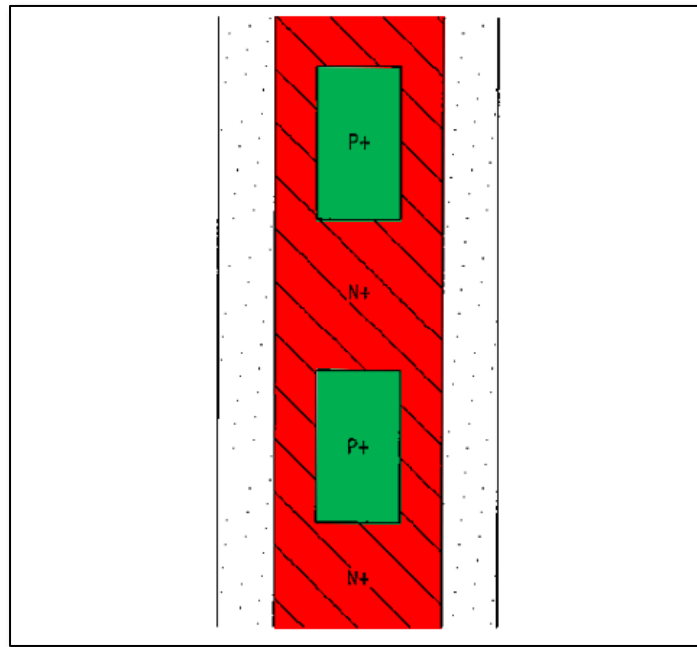
Petition for *Inter Partes* Review  
of U.S. Patent No. 7,498,633

## TABLE OF CONTENTS

	<b>Page</b>
I. INTRODUCTION .....	1
II. MANDATORY NOTICES .....	1
A. Real Party-in-Interest .....	1
B. Related Matters.....	1
C. Counsel .....	2
D. Service Information .....	2
III. LEVEL OF ORDINARY SKILL .....	3
IV. CERTIFICATION OF GROUNDS FOR STANDING .....	3
V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED .....	4
A. Claims for Which Review is Requested and Ground on Which the Challenge is Based .....	4
VI. TECHNOLOGY BACKGROUND.....	4
A. Field-Effect Transistor (“FET”).....	4
B. Power MOSFET .....	7
C. On-Resistance.....	10
D. Unwanted Activation of Parasitic Components—Latch Up .....	12
E. Silicon Carbide (SiC) .....	17
F. Visualizing Three-Dimensional Semiconductor Structures.....	18
VII. OVERVIEW OF THE ’633 PATENT .....	23
A. Alleged Invention .....	23
B. Prosecution History .....	30
VIII. PRIOR ART PATENTS AND PUBLICATIONS .....	32
A. <i>Ryu</i> .....	32
B. <i>Williams</i> .....	37
IX. CLAIM CONSTRUCTION .....	38

Petition for *Inter Partes* Review  
of U.S. Patent No. 7,498,633

X.	SPECIFIC GROUND FOR UNPATENTABILITY .....	39
A.	Ground I: Claims 9–11 are Obvious Over <i>Ryu</i> in View of <i>Williams</i> ..	39
1.	Independent Claim 9 .....	39
2.	Dependent Claim 10 .....	80
3.	Dependent Claim 11 .....	81
XI.	CO-PENDING DISTRICT COURT LITIGATION IN TEXAS SHOULD NOT PRECLUDE INSTITUTION .....	83
A.	The potential for a stay of the district court case urges against denial (factor 1) .....	83
B.	Uncertainty over the trial date in the Texas case favors institution (factor 2) .....	83
C.	Investment in the parallel district court proceeding is minimal and ST was diligent in filing this Petition (factor 3) .....	85
D.	The Petition raises unique issues, which favors institution (factor 4) ..	86
E.	The parties overlap (factor 5) .....	86
F.	The merits of ST’s challenge support institution (factor 6) .....	86
XII.	CONCLUSION.....	87



EX1004, FIG. 19E (annotated)

## IX. CLAIM CONSTRUCTION

During IPR, claims are construed according to the “*Phillips* standard.” *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board need only construe the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, given the close correlation between the asserted prior art and the challenged claims of the ’633 patent, the Board need not construe any terms of the challenged claims to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their plain meaning (as would have been understood by a POSITA

at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.<sup>4</sup>

## **X. SPECIFIC GROUND FOR UNPATENTABILITY**

Under 37 C.F.R. § 42.104(b)(4)–(5), the following sections (as confirmed in Dr. Subramanian’s declaration, EX1002, ¶¶70–143) detail the ground of unpatentability, the limitations of challenged claims 9–11 of the ’633 patent, and how these claims are therefore obvious in view of the prior art. EX1002, ¶¶70–143.

### **A. Ground I: Claims 9–11 are Obvious Over *Ryu* in View of *Williams***

#### **1. Independent Claim 9**

##### ***a) 9[preamble]: “A double-implanted metal-oxide semiconductor field-effect transistor comprising:”***

Regardless of whether the preamble is limiting, *Ryu* discloses it. *Ryu* discloses a metal-oxide semiconductor field-effect transistor (MOSFET). EX1003, ¶¶3, 28, 40. *Ryu* explicitly states that Figure 2A is a MOSFET. *Id.*, ¶40 (“MOSFETs according to embodiments of the present invention are illustrated in FIG. 2A.”). *Ryu*’s Figure 2A is reproduced below, alongside the ’633 patent’s Figure 1 for comparison. EX1002, ¶72.

---

<sup>4</sup> Petitioner reserves all rights to raise claim construction and other arguments in this and other proceedings as relevant and appropriate.

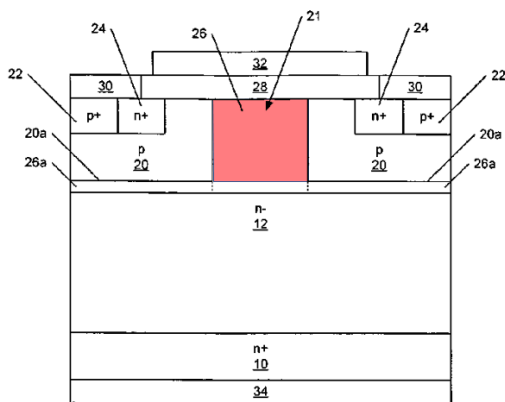
Petition for *Inter Partes* Review  
of U.S. Patent No. 7,498,633

j) **9[i]: “a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.”**

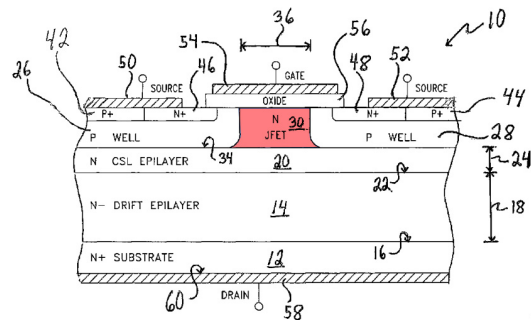
Ryu discloses element 9[i]. As explained below, *Ryu* expressly discloses a “JFET region.” *Ryu*’s “JFET region” is defined between the first and second source regions in the same way as in the ’633 patent. Moreover, *Ryu*’s “JFET region” is disclosed as having a range of width that substantially overlaps with the range of “less than about three micrometers.” EX1002, ¶135.

i. “a JFET region”

*Ryu* expressly discloses that the gap between the p-wells 20 “may be referred to as the **JFET region 21**.” EX1003, ¶44; cf. EX1001, 6:3–5 (“The remaining region of the additional epitaxial layer between the wells 26, 28 forms the JFET region 30.”). *Ryu*’s **JFET region 21** in Figure 2A is shown beside the ’633 patent’s “JFET region” below, both annotated in salmon. EX1002, ¶136.



EX1003, FIG. 2A (annotated)

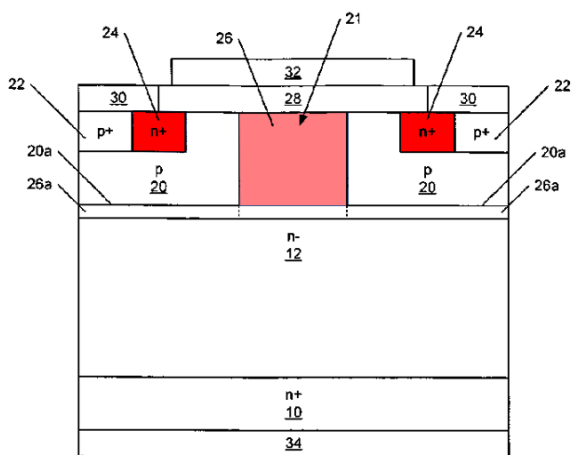


EX1001, FIG. 1 (annotated)

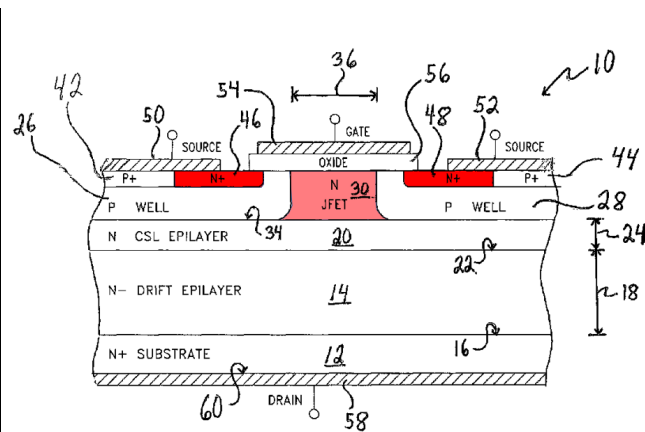
Petition for *Inter Partes* Review  
of U.S. Patent No. 7,498,633

ii. *“defined between the first source region and the second source region”*

Ryu’s **n+ regions 24** (i.e., the “first source region” and “second source region”) are disposed within p-wells 20. And Ryu states that “the region [between the p-wells 20] may be referred to as the JFET region 21.” EX1003, ¶44. The **JFET region 21** is as illustrated in Figure 2A, for example. As such, Ryu discloses that the **JFET region 21** is between the first and second source regions. Also, as shown below, Ryu’s arrangement is identical to that shown in the ’633 patent, where both structures include a portion of each p-well between the JFET region and each source region disposed within each respective p-well. Accordingly, Ryu’s **JFET region 21** is “defined between the first source region and the second source region” in the same way as the ’633 patent’s JFET region. EX1002, ¶137.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)



iii. ***“the JFET region having a width less than about three micrometers”***

Ryu discloses that “if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region 21** may become very high,” and thus “gaps of from about 1  $\mu\text{m}$  to about 10  $\mu\text{m}$  are preferred.” EX1003, ¶44. Thus, Ryu discloses that the **JFET region 21** may have a width of less than about three micrometers because the recited width of “less than about three micrometers” is disclosed with sufficient specificity by Ryu’s disclosure of a JFET width “from about 1 [micrometer] to about 10 [micrometers].” EX1002, ¶138. *See also ClearValue Inc. v. Pearl River Polymers Inc.*, 668 F.3d 1340, 1345, 101 USPQ2d 1773, 1777 (Fed. Cir. 2012) (finding a claimed narrow range was disclosed with “sufficient specificity” by a reference disclosing a broader range where, like here, there was “no ‘considerable difference between the claimed range and the range in the prior art.’” (internal citations omitted)).

Therefore, Ryu in view of *Williams* renders claim 9 obvious. *Id.*, ¶139.

## 2. Dependent Claim 10

***“The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a width of about one micrometer.”***

Ryu in view of *Williams* renders obvious claim 9, as discussed above. Ryu discloses the additional limitation of claim 10. For example, Ryu discloses that “if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region**

Petition for *Inter Partes Review*  
of U.S. Patent No. 7,498,633

**CERTIFICATE UNDER 37 CFR § 42.24(d)**

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes Review* totals 13,648, which is less than the 14,000 words allowed under 37 CFR § 42.24(a)(1)(i).

Respectfully submitted,

Dated: December 6, 2021

/Scott Bertulli/  
Scott Bertulli  
Reg. No. 75,886

Petition for *Inter Partes* Review  
of U.S. Patent No. 7,498,633

**CERTIFICATE OF SERVICE**

I hereby certify that on December 6, 2021, I caused a true and correct copy of  
the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,498,633 under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibit List
- Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 7,498,633 (EX1001–EX1028)
- Power of Attorney
- Fee Authorization
- Word Count Certification Under 37 CFR § 42.24(d)

to be served via Express Mail on the following correspondent of record as listed on  
PAIR:

Barnes & Thornburg LLP  
11 S. Meridian Street  
Indianapolis IN 46204

DATED: December 6, 2021

/Scott Bertulli/  
Scott Bertulli  
Reg. No. 75,886